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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,215	08/20/2003	Darel N. Emmot	10001763-1	5465

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EXAMINER	
TUNG, KEE M	
ART UNIT	**PAPER NUMBER**
2671	

DATE MAILED: 08/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,215	EMMOT ET AL.	
	Examiner	Art Unit	
	Kee M. Tung	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The response filed 6/24/05 has been considered in preparing this office action.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "partitioning logic" (claims 7 and 10-11) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nelson et al (6,801,202 hereinafter "Nelson") in view of Spencer (6,311,247).

Nelson teaches a computer system (Figs. 2 and 3) comprising a host processor (102) configured to execute a single-threaded application; partitioning logic (such as, control unit 140 for dividing the stream of data received from computer system 80 into a corresponding number of parallel stream, col. 9, lines 20-24; and Fig. 22) for partitioning the state-sequenced information, communication logic (not shown, but can be any bus connectivity logic, such as, crossbar, chipset or bridge, see col. 8, lines 13-20, such as, arbiter in control unit of Fig. 22) configured to communicate partitioned state-sequenced information across a plurality of I/O busses (shows one bus, but could be multiple separate busses since Nelson suggests one or more graphics processor 90, see col. 9, line 1, further see Spencer for the teachings of multiple busses); a plurality of interfaces (bus arbiter) located at a subsystem (112) for receiving the information communicated across the plurality of I/O busses; processing logic (graphics processor 90 in Fig. 3) for controlling the processing of the partitioned information without re-sequencing the information, the processing logic configured to preserve state information of the information processed. However, Nelson fails to explicitly teach a plurality of I/O

busses. This is what Spencer teaches. Spencer teaches a computer system (Fig. 2) comprising a host processor (112) configured to execute a single-threaded application; partitioning logic (123) for partitioning the state-sequenced information, communication logic (chipset 120) configured to communicate partitioned state-sequenced information across a plurality of I/O busses (PCI buses 116-118); a plurality of interfaces (124-128) located at a subsystem for receiving the information communicated across the plurality of I/O busses; processing logic (not shown, but would have been obvious to connect any peripheral (I/O) devices into the PCI busses 116-118, for example, graphics processor is considered one of the peripheral device) for controlling the processing of the partitioned information without re-sequencing the information, the processing logic configured to preserve state information of the information processed. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of separate multiple I/O or PCI busses into the system of Nelson in order to replace the single bus system of Nelson by the multiple busses of Spencer because multiple separate busses allows exclusive communication by providing a direct pipe therebetween and thus provides significant performance enhancements over prior art systems that have shared PCI busses as taught by Spencer (abstract). Therefore, at least claims 7, 9, 10, 12 and 14 would have been obvious.

As per claim 8, Spencer teaches a buffer memory (Fig. 4, cache 150) in communication with the host processor for storing state-sequenced information for communication to a subsystem.

As per claim 11, Spencer teaches the partitioning logic is located in at the host processor (Fig. 2, chipset 120).

As per claim 13, Nelson teaches the processing logic comprises at least one geometry accelerator (112).

As per claim 15, the combined system teaches the system comprises a plurality of processing nodes that are coupled through a communication network (Nelson, one or more graphics processor, col. 9, line 1 and Spencer, PCI devices connect into the PCI busses 116-118).

Method claims 1, 2 and 4-6 are similar in scope to system claims 7-15 above, and thus are rejected under similar rationale.

As per claim 3, Nelson teaches the communicating partitioned state-sequenced information comprises performing at least one DMA across each of the plurality of I/O busses (col. 8, lines 26-31).

4. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nelson et al (6,801,202 hereinafter "Nelson") and Spencer (6,311,247) as applied to claims 7 and 15 above, and further in view of Ebihara et al (6,924,807 hereinafter "Ebihara").

The teachings of Nelson and Spencer are given in previous paragraph of this Office action. However, the combined system fails to explicitly teach the processing logic comprises work queues maintained among the processing nodes. This is what Ebihara teaches. Ebihara teaches an image processing apparatus comprising a plurality of graphics processors (104), each being operable to render the image data (110) and at least one merge unit (106) operable to synchronously (108 or 118) receive

the image data and synchronously (108 or 118) produce combined frame image data based thereon (abstract, Fig. 3). The Synchronous unit (108) performs similar functions as the work queue which provides synchronization among plurality of graphics processor. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the synchron unit (108 or 118) into the combined system in order to provide synchronization among multiple graphics processors and thus to provide synchronized output signals. Therefore, at least claim 16 would have been obvious.

Response to Arguments

5. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M. Tung whose telephone number is 571-272-7794. The examiner can normally be reached on Tuesday - Friday from 5:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kee M Tung
Primary Examiner
Art Unit 2671